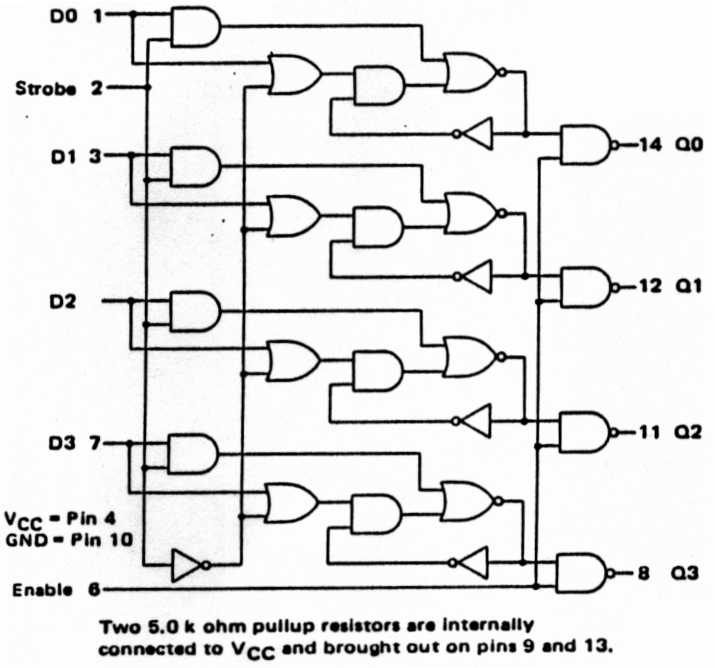
LANSDALE Semiconductor, Inc.

ML4335
Quad Latch
(Open Collector)

Legacy Device: *Motorola MC4335*



This monolithic device consists of four latch circuits with open collector outputs common Strobe input, and output enable input. The output of each latch will follow the data input when the Strobe input is in a logical “1” state. When the Strobe is in a logical “0” state, the latch will store the logic state of the data input just prior to the change of the Strobe from a “1” level to a “0” level.

The open collector outputs make this device useful for bussing or wire ORing outputs together. Two 5.0 k ohm resistor are available in the package to provide the passive pullup function in wired–OR or bussed operation. The output enable is useful where it is desirable to gate information out of the latches according to a predetermined timing scheme.

Input Loading Factor (MTTL 1 Loads):

Data Input (Strobe High) – 4335 = 4.2

Data Input (Strobe Low) – 4335 = 1.1

Output Enable – 4335 = 4.0

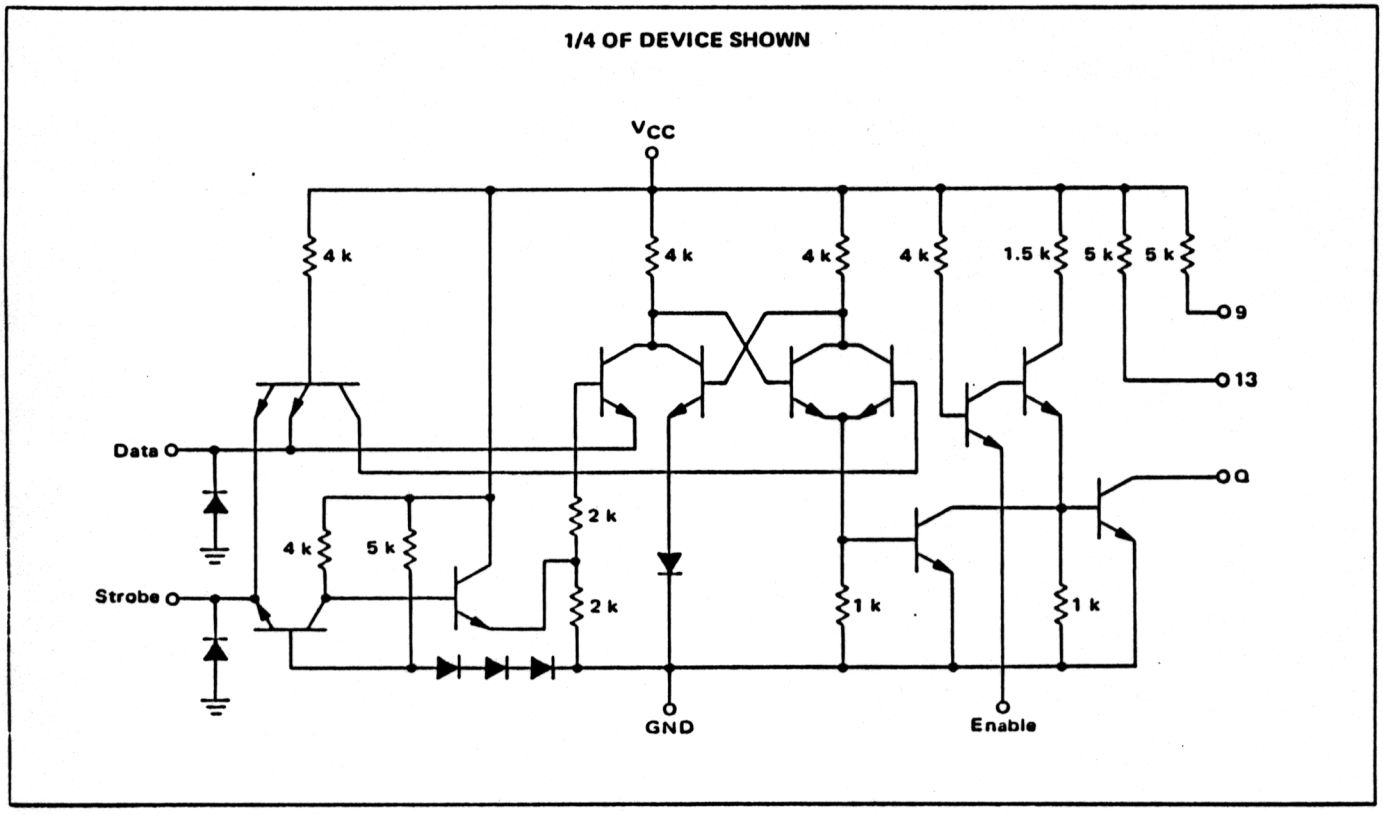
Output Loading Factor (TTL 1 Loads):

4335 = 7 (1OL = 9.3 mAdc)

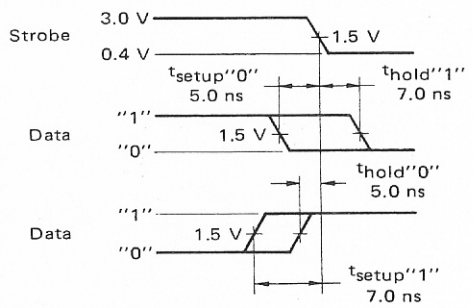
Total Power Dissipation = 140 mW typ/pkg

Propegation Delay Time - 25 ns typ

CIRCUIT SCHEMATIC



This quad latch consists of four gated latches that store data on the negative edge of the strobe input. Information must be present at the data inputs prior to the setup time and remain at the data inputs through the hold time to insure that it will be stored by the latch when the negative edge of the strobe occurs. The setup time is 7.0 ns for a logical "1" and 5.0 ns for a logical "0". Hold time is 7.0 ns after the strobe edge for a logical "1" and 5.0 ns prior to the strobe edge for a logical "0".



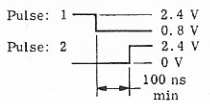
ELECTRICAL CHARACTERISTICS

Test procedures are shown for the Strobe, Enable, and only one data input, and for one output. Other data inputs and outputs are tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC4335 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Input									
Forward Current	I_F	1	-	-5.6	-	-5.6	-	-5.6	mAdc
		1	-	-1.5	-	-1.5	-	-1.5	
		2	-	-7.0	-	-7.0	-	-7.0	
		6	-	-5.3	-	-5.3	-	-5.3	
		13	-	-1.3	-	-1.3	-	-1.3	
Leakage Current	I_R	1	-	0.2	-	0.2	-	0.2	mAdc
		2	-	0.5	-	0.5	-	0.5	
		6	-	0.4	-	0.4	-	0.4	
Breakdown Voltage	BV_{in}	1	5.5	-	5.5	-	5.5	-	Vdc
		2		-		-		-	
		6		-		-		-	
Output									
Output Voltage	V_{OL}	14	-	0.4	-	0.4	-	0.4	Vdc
		14	-		-		-		
		14	-		-		-		
	V_{OH}	14	2.4	-	2.4	-	2.4	-	Vdc
		14	2.4	-	2.4	-	2.4	-	Vdc
Leakage Current	I_{CEX}	14	-	0.25	-	0.25	-	0.25	mAdc
		14	-	1.0	-	1.0	-	1.0	mAdc
Power Requirements (Total Device)									
Maximum Power Supply Current	I_{max}	4	-	-	-	44	-	-	mAdc
Power Supply Drain	I_{PDH}	4	-	42	-	42	-	42	mAdc
	I_{PDL}	4	-	34	-	34	-	34	mAdc

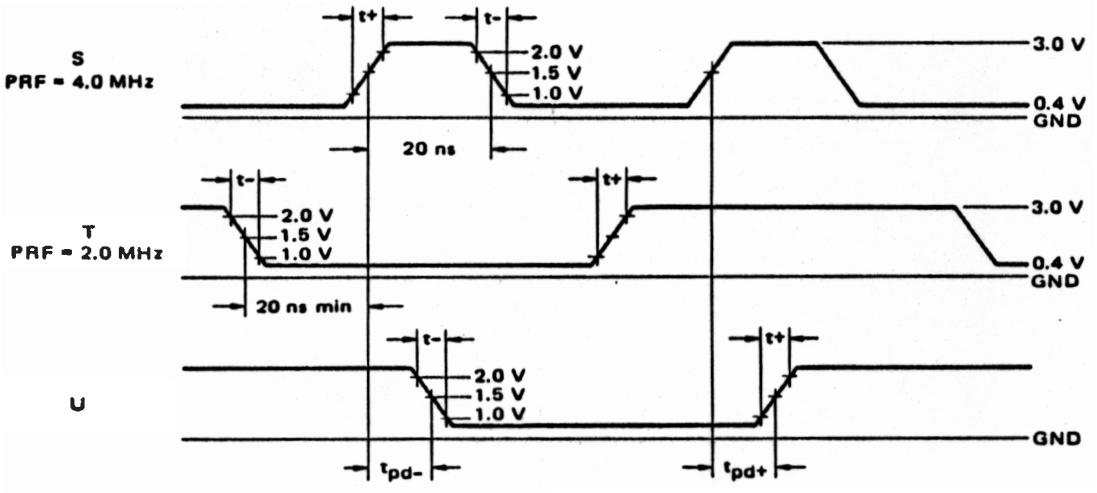
TEST CURRENT/VOLTAGE VALUES (All Temperatures)												
mA			Volts									
I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_F	V_R	V_{out}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	
11.6	0.1	1.0	0.8	2.0	0.4	4.5	5.5	7.0	5.0	4.5	5.5	

TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:														
I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_F	V_R	V_{out}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	Pulse 1	Pulse 2	Gnd
					1	2					4			10
			2		1	3,5,7								
					2	1,3,5,6,7								
					6	1,2,3,5,7								
					13	1								
						1					4			2,10
						2								1,3,5,7,10
						6								1,2,3,5,7,10
		1									4			2,10
		2												1,3,5,6,7,10
		6												1,2,3,5,7,10
14				6		2,3,5,7				4				1,10
14			1	2,6										10
14												2	1	10
	14		6			2				4				1,3,5,7,10
	14			1,2,6						4				10
						1,2	14				4			10
								14	4					6,10
						2		4						1,3,5,6,7,10
									4					10
									4					1,3,5,6,7,10

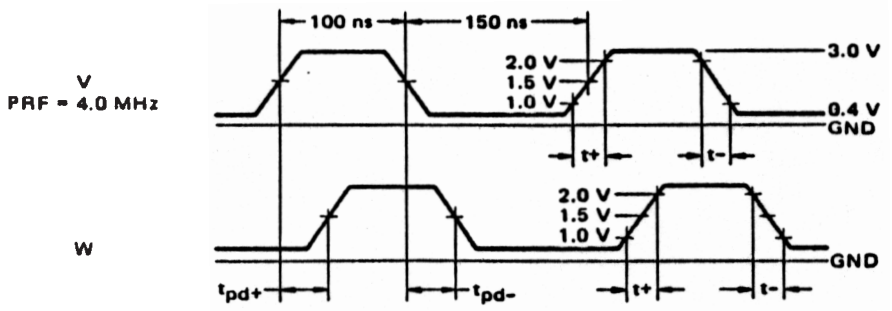


VOLTAGE WAVEFORMS

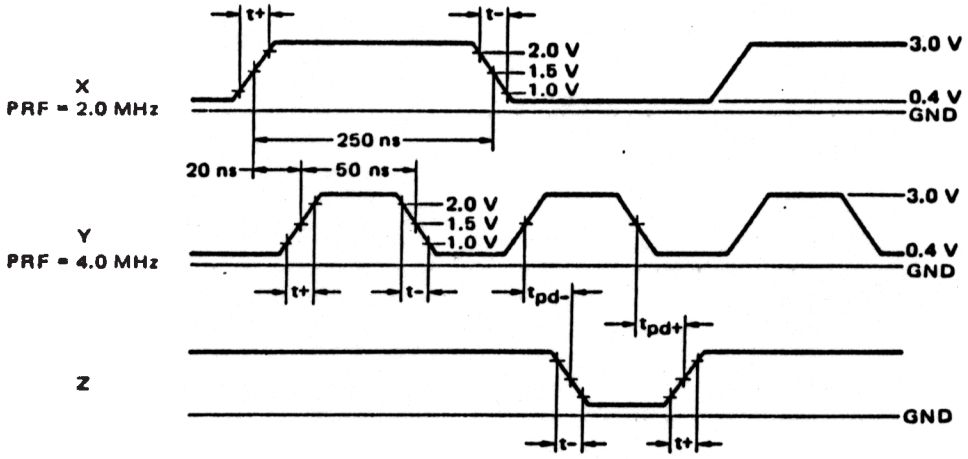
Strobe Input



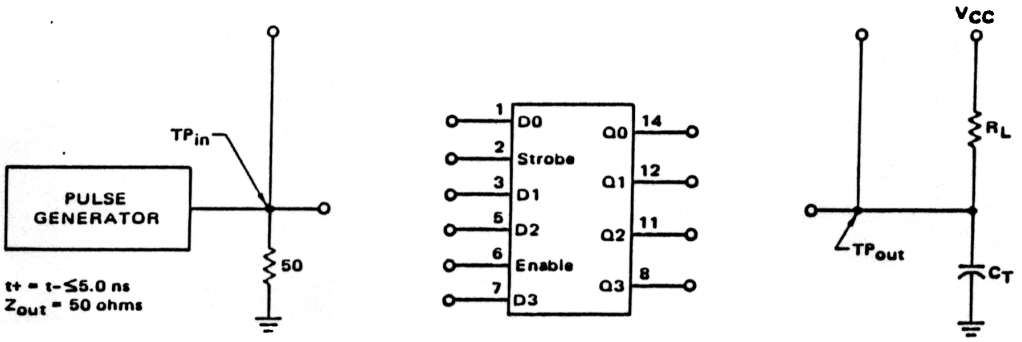
Data Inputs



Enable Inputs



SWITCHING TIME TEST CIRCUIT



Two pulse generators are required and must be slaved to provide the waveforms shown.

R_L value given in Switching Time Test Procedures table.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

High impedance probes (>1.0 Megohm) must be used.

SWITCHING TIME TEST PROCEDURES (T_A = 25°C)

(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	PIN UNDER TEST (In/Out)	INPUT Pin 1 D0	INPUT Pin 2 Strobe	INPUT Pin 6 Enable	OUTPUT Pin 14 D0	R_L Ohms 4335	LIMITS (ns) Max 4335
Strobe Propagation Delay	t_{pd+1}	2/14	T	S	2.4 V	U	510	25
	t_{pd-1}	2/14	T	S	2.4 V	U	510	40
	t_{pd+2}	2/14	T	S	2.4 V	U	5.0 k	50
	t_{pd-2}	2/14	T	S	2.4 V	U	5.0 k	34
Rise Time	t+	14	T	S	2.4 V	U	510 or 5.0 k	0.3 RC
Fall Time	t-	14	T	S	2.4 V	U	510	9.0
Data Propagation Delay	t_{pd+3}	1/14	V	2.4 V	2.4 V	W	510	20
	t_{pd-3}	1/14	V	2.4 V	2.4 V	W	510	30
	t_{pd+4}	1/14	V	2.4 V	2.4 V	W	5.0 k	50
	t_{pd-4}	1/14	V	2.4 V	2.4 V	W	5.0 k	25
Enable Propagation Delay	t_{pd+3}	1/14	X	2.4 V	Y	Z	510	20
	t_{pd-3}	1/14	X	2.4 V	Y	Z	510	30
	t_{pd+4}	1/14	X	2.4 V	Y	Z	5.0 k	50
	t_{pd-4}	1/14	X	2.4 V	Y	Z	5.0 k	25
Minimum Strobe Enable	–	1/14	T ①	1.8 V	2.4 V	②	5.0 k	②
Maximum Strobe Inhibit	–	1/14	T ①	1.0 V	2.4 V	③	5.0 k	③

① Pulse T conditions changed: V_L = 1.0 V, V_H = 1.8 V
② Output shall follow data input.
③ Output shall not toggle.